100 MHz to 17 GHz Dual-Gate Variable-Gain Amplifier

N. MAMODALY, P. QUENTIN, P. DUEME, AND J. OGREGON

Abstract — **A simple analytical approach to wide-band amplification using commercially available dual-gate FET's has enabled an ultra-wide-band flat-gain amplifier to be built in the 100-MHz to 17-GHz bandwidth, with a VSWR less than 3.5- and 15-dB gain control. A description is given, including first experimental results.**

I. Introduction

In very broad-band amplifiers, variable gain stages are needed to compensate the variation of the other stages, particularly versus temperature. The gain control can be achieved by p-i-n diodes with variable losses, or by dual-gate FET's with variable gain.

We present here an ultra-broad-band variable gain unit giving 15-dB variation in the 100-MHz to 17-GHz bandwith a VSWR less than 3.5.

II. Theoretical Design

Recently, ultra-broad-band single-gate FET stages have been designed using *R-L* equalization networks [1], [2]. The same design can be applied to dual-gate stages, considering a two-port equivalent network (between gate 1 and drain). It can be shown that, when the second gate is ac grounded, with a variable dc bias voltage between 0V and -2V, S_{11} and S_{22} parameters do not show significant variations for the NEC 463 measured in chip form [3]. We can develop from S parameter measurements a simplified equivalent circuit (Fig. 1). Using this equivalent circuit, a variable gain stage is design with *R-L* equalization networks.

In our model, an FET can be described by the product of three transfer functions, one of them (including G_m) being constant. The two others, describing the input and output circuit of the FET, are of second-order type versus frequency. Theoretically, in order to obtain a flat gain from zero to $F_{\max}$, each circuit must be tuned at $F_{\max}$ and transformers must be used so that the input and output circuits have Q-factors equal to unity at $F_{\max}$ [1], [3].

In order to match the amplifier to 50 Ω, a simple resistance in series with an inductance is included at the input and output of each transistor in parallel with the second-order circuits previously described (Fig. 2). An approximate value of these matching networks can be obtained analytically and finally computer optimized.

III. Experimental Results

Experimental amplifiers have been realized with NEC 463 FET's. Fig. 2 shows the overall circuit under test. The first FET is bias adjusted (VGS_1, VGS_2) to optimize flat gain. The bias of gate 2 of the second FET controls the gain of the amplifier in a 15-dB range. Fig. 3 indicates the gain, and input and output VSWR of a two-stage amplifier. For $VSG_{2B} = 0$ V, the gain is $+5$ dB and goes down to -13 dB for a $VGS_{2B} = -1.7$ V from 100 MHz to 17 GHz. Input VSWR is lower than 3.5 and output VSWR is lower than 2.5 in the bandwidth.

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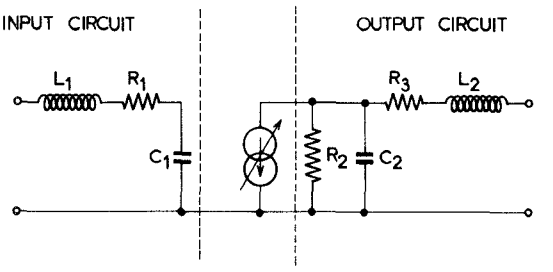

Fig. 1. Simplified FET model. 15.6 mΩ $< G_m <$ 0.9 mΩ. 0 V $< V_{GS_2} < -2$ V

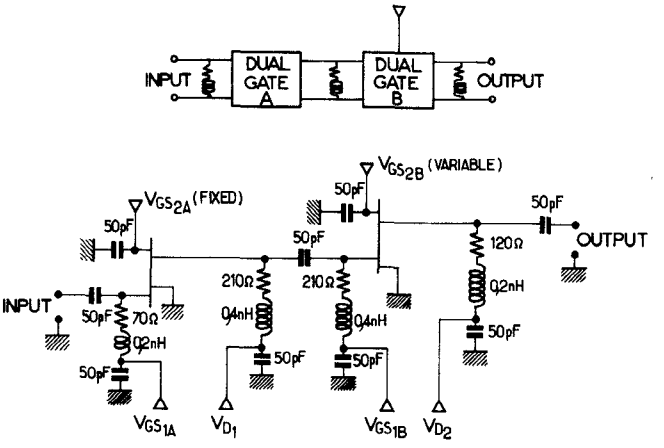

Fig. 2. Dual-gate variable gain amplifier.

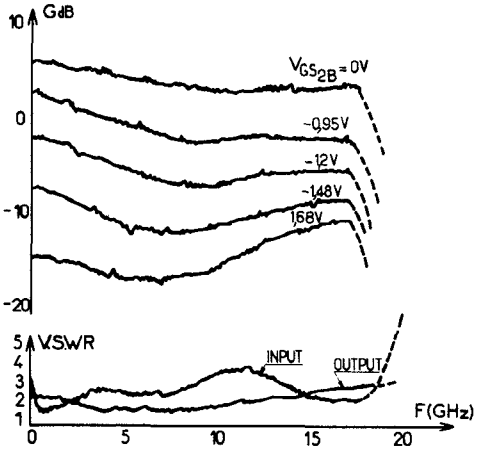

Fig. 3. Two-stage dual-gate amplifier· Gain and VSWR.

IV. Conclusions

An ultra-broad-band variable gain amplifier has been designed, using dual-gate FET's and lumped circuits. The flat gain is controlled in a 15-dB range (between $+5$ dB and -13 dB) with an input and output VSWR lower than 3.5 from 100 MHz to 17 GHz.

This amplifier may conveniently replace the p-i-n diodes stages presently used in broad-band amplifiers.

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Comparison of Single- and Dual-Gate FET Frequency Doublers

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Abstract—**The performance of single- and dual-gate FET frequency doublers is studied by analysis and computer simulation. The theoretical predictions are in good agreement with experimental results. It is shown that the superior performance of the dual-gate FET doubler is largely due to the higher intrinsic gain of the active device.**

I. INTRODUCTION

FET frequency doublers offer the dual attractions of conversion gain and broad-band operating capability at microwave frequencies. Experimental results for single- [1] and dual-gate [2], [3] FET doublers show that the latter offer superior conversion gain. The object of this paper is to compare the performance of single- and dual-gate doublers by means of analysis and computer simulations.

Four major sources of nonlinearity contribute to harmonic generation in both single- and dual-gate FET's:

1) The gate–source junction nonlinear capacitance;

2) The output slope conductance nonlinearity;

3) The clipping of the drain current I_d due to pinchoff, saturation, and gate–source junction forward conduction;

4) The $V_{gs}-I_d$ transfer characteristic nonlinearity.

The effect of each of these nonlinearities on harmonic generation will be discussed in turn, for each type of FET.

II. SINGLE-GATE FET DOUBLER

The nonlinear gate–source junction capacitance has, in general, a large associated series resistance, and efficient harmonic generation using the reverse biased gate–source junction is not possible [4]. The output slope conductance nonlinearity of a typical FET has been shown to be insufficient to make a significant contribution to harmonic generation [5]. When the device gate is biased close to pinchoff or forward conduction, the drain current I_d takes on a half-wave rectified form. The second harmonic component of a half-wave rectified sine wave is 7.4 dB below the corresponding fundamental frequency component, and thus, in the absence of other nonlinearities, the second-harmonic power output would be expected to be of similar magnitude (6 to 8 dB below the fundamental). With the device biased midway between pinchoff and forward conduction, the $V_{gs}-I_d$ characteristic, of the quadratic form $(1-(V_{gs}/V_p))^2$ where V_p is the pinchoff voltage, contributes a maximum second harmonic component level of 12 dB below the corresponding fundamental component at the output. Thus, frequency doubler conversion gain is at best about 6 dB below the corresponding fundamental frequency gain for gate biases close to V_p and 0 V, and somewhat less for biases between these limits. High drive levels cause symmetrical clipping of the I_d waveform due to both pinchoff and gate forward conduction, leading to reduced doubler conversion gain. These simple analytical considerations are supported by results from a large signal computer simulation based on a circuit model for the FET [5]. Fig. 1 compares simulation and experimental results for the dependence of doubler output on gate bias voltage. The experimental results were obtained for a commercial C-band medium power device (MSC 88001) in a test arrangement similar to one described previously [1], the input frequency being 4 GHz.

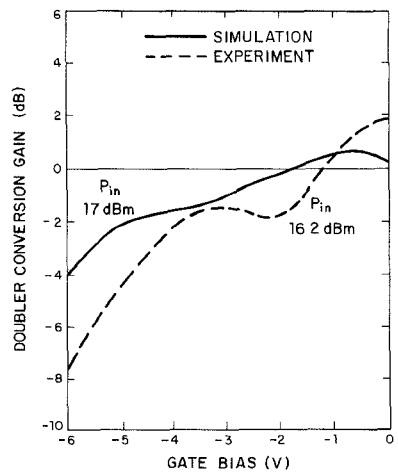

Fig. 1. Comparison of experimental and computer simulation results for a single-gate FET (MSC 88001) frequency doubler. $V_{ds}=5$ V, input frequency $f_{in}=4$ GHz.

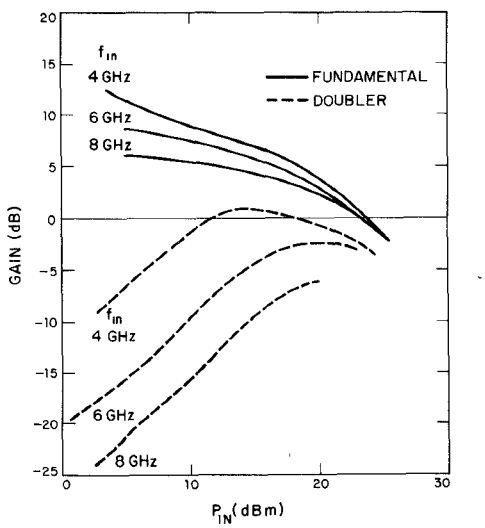

Fig. 2 Computed variation in fundamental and doubler conversion gain with frequency and drive level for a single-gate FET (MSC 88001) $V_{ds}=5$ V, $V_{gs}=0$ V.

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